Combinatorial Analysis of the Reliability of Multi-core Processors

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***Abstract* — The demand for reliability in multi-core processors, which are ubiquitous in today's computers, smartphones, and various other smart devices, is growing. Several factors can influence the seamless operation of multi-core processors. For instance, at high frequencies, challenges such as signal distribution and maintaining low power consumption are prominent. An overheated processor can result in various issues in a computer, including freezes, unexpected shutdowns, and errors while running programs. These issues can have serious consequences, particularly during critical tasks. Processor cores belong to the class of multifunctional elements. Their multifunctionality contributes to the structural flexibility of the processor, allowing functions to be redistributed between cores and ensuring the processor can continue to operate successfully even if individual core blocks fail. This flexibility significantly enhances processor reliability, as demonstrated by quantitative assessments of the fault tolerance of multi-core processors, which is the central focus of this article.**

***Keywords* — Multicore processors, Combinatorial analysis, Multifunctional elements, Reliability, Flexibility.**

I. INTRODUCTION

Enhancing both the performance and reliability are important features of processors. Historically, the progression of computer technology has been propelled by the ability to integrate an increasing number of transistors in circuits. However, a further increase in the performance of processors through the improvement of the technological process of their manufacture is unlikely in the near future. A further significant increase in processor performance is possible only with new architectural solutions under existing technologies. A significant increase in processor performance is possible using the principle of asynchrony [1], although the realization of this idea is unlikely in the near future, as it requires fundamental changes in both the hardware and software areas of the computer.

In order to increase the performance of the processor, designers turn to architectures of parallel operation. Parallelism can be implemented at different levels. At the lowest level, it can be realized at the expense of convolution and superscalar architecture in the processor core. In this case, the processor core has several functional blocks and the parallel execution of commands is based on the parallel processing of several threads.

The next level of parallelism is achieved through multi-core architecture, where multiple processor cores are integrated into a single crystal or unit, operating in parallel. The implementation of numerous cores within multi-core processors is effective particularly when complex tasks are performed in parallel [2]. However, parallel architectures, in addition to increasing the performance of the processor, offer great opportunities in terms of increasing the reliability of the processor. The multi-core and parallel computing capabilities of the processors create a prerequisite for increasing the failure-resistanting and reliability of the processors. For instance, in the event of a functional block failure within one processor core, its functions can seamlessly transfer to a corresponding block within another core, enabling uninterrupted processor operation [3], [4]. In this case, mathematical modeling and analysis of the described process is interesting and important.

II. COMBINATORIAL ANALYSIS

It is preferable to use combinatorial analysis methods to calculate the probabilities of falsehoods associated with individual blocks in a multi-core processor. Let us consider a processor core model with four executive (functional) blocks: an arithmetic-logic device, two blocks for accessing memory, one block performing operations on floating-point numbers, which independently of each other, perform the corresponding type of operations in parallel (see Fig. 1).

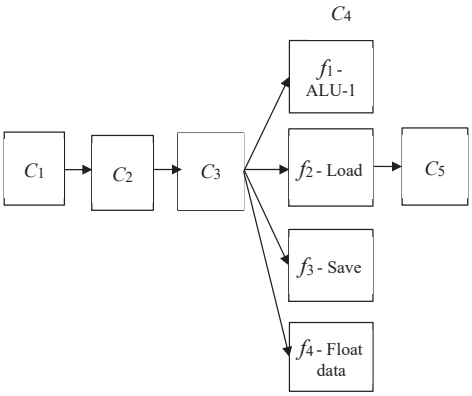

Fig. 1. Superscalar processor core with four execution blocks.

In the Fig. 1, C_1 represents command selection block, C_2 - decoding block, C_3 - operand selection block, C_4 – functional block and C_5 - the block of writing in registers.

It is supposed that the processor is in a state of marginal performance-ability if the functions of all four execution blocks are performed in its cores. Even a single block failure causes the processor to fail. With such an assumption, the shortest ways of functioning of an n-core processor can be described by the following logical function (conjunctions):

$$S_q = a_{i1}(f_1)\ \&\ a_{i2}(f_2)\ \&\ \cdots\ \&\ a_{im}(f_m) = 1,$$

where a_i denotes i-th block, $i_1,\ i_2, \cdots,\ i_m \in [1, n],\ \ q \in [1, N_S],\ N_S = 2^m$.

The condition of the processor's performance-ability is written by the disjunction of the ways of functioning:

$$F_A[a_1(f_1), a_2(f_2), \cdots, a_n(f_m)] = \bigcup_{q=1}^{N_S} S_q.$$

If we consider the example of the core given in Fig. 1, then a 2-core processor of class $n = 2, m = 4$ with 4 operational blocks can be described by the following (0,1) matrix:

$$B_A[a_i(f_j)] = \left\| \begin{matrix} a_1(f_1) & a_1(f_2) & a_1(f_3) & a_1(f_4) \\ a_2(f_1) & a_2(f_2) & a_2(f_3) & a_2(f_4) \end{matrix} \right\|$$

where $a_i(f_j) = 1$ if j block of a_i core performs f_j function and $a_i(f_j) = 0$, in opposite case.

If we introduce notations:

$$a_1(f_1) = x_1,\ a_1(f_2) = x_2,\ \ a_1(f_3) = x_3,$$
$$a_1(f_4) = x_4,\ a_2(f_1) = x_5,\ a_2(f_2) = x_6,$$
$$a_2(f_3) = x_7,\ \ a_2(f_4) = x_8,$$

then the shortest paths for the operation of a 2-core processor are written by the following conjunctions:

$$S_1 = x_1x_2x_3x_4,\ S_2 = x_1x_2x_3x_8,\ S_3 = x_1x_2x_4x_7,$$
$$S_4 = x_1x_3x_4x_6,\ S_5 = x_2x_3x_4x_5,\ S_6 = x_1x_2x_7x_8,$$
$$S_7 = x_1x_3x_6x_8,\ S_8 = x_2x_3x_5x_8,\ S_9 = x_1x_4x_6x_7,$$
$$S_{10} = x_2x_4x_5x_7,\ S_{11} = x_3x_4x_5x_6,\ S_{12} = x_1x_6x_7x_8,$$
$$S_{13} = x_2x_5x_7x_8,\ S_{14} = x_3x_5x_6x_8,\ S_{15} = x_4x_5x_6x_7,$$
$$S_{16} = x_5x_6x_7x_8.$$

The same ways of functioning with (0,1) logical variables are given in Table 1:

Table 1

	a_1				a_2			
A/F	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8
X	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8
1	1	1	1	1	0	0	0	0
2	1	1	1	0	0	0	0	1
3	1	1	0	1	0	0	1	0
4	1	0	1	1	0	1	0	0
5	0	1	1	1	1	0	0	0
6	1	1	0	0	0	0	1	1
7	1	0	1	0	0	1	0	1
8	0	1	1	0	1	0	0	1
9	1	0	0	1	0	1	1	0
10	0	1	0	1	1	0	1	0
11	0	0	1	1	1	1	0	0
12	1	0	0	0	0	1	1	1
13	0	1	0	0	1	0	1	1
14	0	0	1	0	1	1	0	1
15	0	0	0	1	1	1	1	0
16	0	0	0	0	1	1	1	1

Using our application based on combinatorial analysis and logical-probabilistic methods, the following results were obtained:

- When $p_i = 0.99$, where p_i - is the probability of the functionality of each functional block, the probability of the processor's faultlessness is $P(A_F) = 0.9996$;
- The number of all possible states - $N_\Omega = 2^{nm} = 2^8 = 256$;
- The number of operational states - $N_R = 81$;
- The coefficient of structural perfection of the processor - $\eta_A = N_R/N_\Omega = 0.31640625$.

The same result of η_A ($\eta_A = 0.31640625$) is obtained if we insert into the reliability polynomial the probability of operation of each functional block $p_i = 0.5$.

For the purpose of comparative analysis, let us consider a 4-core processor of class $n = m = 4$, in which each core contains 4 functional blocks. We consider the limiting case when in each core operates one block in different combinations so as to ensure the operation of all four executing blocks at the same time [5].

In such a case, when $n = m = 4$, the functional resource matrix of the processor will be $B_A(4 \times 4) = [a_i(f_j)]$, and the shortest paths of operation will be written by the following logical function [4], [6], [7]:

$$S_q = a_1(f_{j1})\ \&\ a_2(f_{j2})\ \&\ a_3(f_{j3})\ \&\ a_4(f_{j4}) = 1,$$

where

$$j_1,\ j_2,\ j_3,\ j_4 \in [1,4],\ \ j_1 \neq j_2 \neq j_3 \neq j_4,$$
$$q \in [1, N_S], \qquad N_S = 4! = 24.$$

The results of calculations performed by combinatorial analysis methods are presented in Table 2.

Table 2

γ	$N_M(n,\gamma)$	$N_L(n,\gamma)$	$g_A(\gamma)$
0	1	1	1
1	16	16	1
2	120	120	1
3	560	560	1
4	1820	1812	0.9956
5	4368	4272	0.9780
6	8008	7432	0.9281
7	11440	9312	0.8140
8	12870	8010	0.6224
9	11440	4464	0.3902
10	8008	1512	0.1888
11	4368	288	0.0659
12	1820	24	0.0132
13	560	0	0
14	120	0	0
15	16	0	0
16	1	0	0
Σ	$N_\Omega = 65536$	$N_R = 37823$	$\eta_A = 0.57713$

In Table 2:

- γ is a number of functional blocks out of order in the processor, $\gamma \in [0,16]$;
- $N_M(n,\gamma)$ is a number of all possible states with γ number of failures, $N_\Omega = 2^{16} = 65536$;
- $N_L(n,\gamma)$ is a number of operational states with γ number of failures;
- $g_A(\gamma)$ is a processor's failure-resistanting coefficient with γ number of failures.

III. CONCLUSION

Based on our evaluation of the reliability indicators of the multi-core processor, several conclusions can be drawn:

1. The expansion of the processor's core count correlates with an increase in the number of shortest operation paths N_S, thereby enhancing the flexibility of the system's structure and maneuverability of the system.
2. Augmenting the core count substantially amplifies both the total number of possible operational states N_Ω and the number of states impacting the processor's performance N_R.
3. With a rise in the number of processor cores, there is a notable escalation in the proportion of performance states relative to all possible states, indicating a higher structural perfection index η_A for the processor.

Concurrently with the core count increment, there is a marked increase in the likelihood of the processor functioning without a malfunction and a failure resistance rate.

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